Reconfigurable Biologically Inspired Visual Motion Systems Using Modular Neuromorphic VLSI Chips

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***Abstract*—Visual motion information provides a variety of clues that enable biological organisms from insects to primates to efficiently navigate in unstructured environments. We present modular mixed-signal very large-scale integration (VLSI) implementations of the three most prominent biological models of visual motion detection. A novel feature of these designs is the use of spike integration circuitry to implement the necessary temporal filtering. We show how such modular VLSI building blocks make it possible to build highly powerful and flexible vision systems. These three biomimetic motion algorithms are fully characterized and compared in performance. The visual motion detection models are each implemented on separate VLSI chips, but utilize a common silicon retina chip to transmit changes in contrast, and thus four separate mixed-signal VLSI designs are described. Characterization results of these sensors show that each has a saturating response to contrast to moving stimuli, and that the direction of motion of a sinusoidal grating can be detected down to less than 5% contrast, and over more than an order of magnitude in velocity, while retaining modest power consumption.**

***Index Terms*—Address-Event Representation (AER), analog very large-scale integration (VLSI), biomimetic, modular, neuromorphic, visual motion.**

I. Introduction

THE REAL-TIME processing of visual motion is very compute-intensive and is limited in small autonomous robots and embedded systems by issues of size, weight, and electrical power consumption. Conventional design approaches to image processing that employ a charge-coupled device (CCD) camera delivering high-speed frames of visual information together with a serial discrete-time digital signal processor are not architecturally well matched to, and thus not efficient for, visual motion processing which can be computed in parallel using nearest neighbor communication only.

A direct implementation of visual motion processing algorithms using analog pixel-parallel computation with nearest neighbor communication can efficiently compute motion in real time, and this has been an active area of research for nearly two decades [1]–[15]. Biologically inspired algorithms which compute the spatio-temporal frequency (STF) content in each local patch of the image have significant advantages over optical-flow based representations. Since each sensor only detects the STF content of the signal, multiple motions (distinguished in spatial or temporal frequency) can be represented in a single local image region by using a bank of such sensors with different spatial and temporal frequency tunings. Additionally, the lack of a digital threshold at any point in the algorithm means that detection of motion at low contrast or low speed requires only a sufficient temporal integration time to average out noise. These issues are discussed at greater length in a related paper [16] in which the same three STF-based algorithms utilized in this paper are described in monolithic analog very large-scale integration (VLSI) implementations.

Monolithic focal plane motion sensors have the advantage over multichip approaches that the image data is transduced and processed in the focal plane and need not be communicated to a separate processor. One drawback of this approach is that, the more complex the motion computation becomes, the lower the fill factor (the percentage of pixel area dedicated to phototransduction) becomes [17]. In order to prevent the fill factor from becoming unacceptably small, we can partition the motion computation into two tightly coupled custom VLSI chips. However, in order for the motion computation to be partitioned without dramatically increasing power consumption, it is essential that the stream of information flowing from the phototransduction stage be reduced over that from a CCD imager. We accomplish this by having the chip incorporating phototransduction (termed the *sender chip*) only transmit changes in local luminance. The two-dimensional (2-D) spatial position of these changes is transmitted over an asynchronous digital bus [18] to achieve low average power consumption. A motion processor (the *receiver chip*) uses this luminance change information to compute a 2-D array of local motion information. Fig. 1 outlines some of the possibilities for complex motion computations with these two chips; see [17] for details and characterizations of previous generations of such systems. Note that the computation in this system is *data driven*, since nothing happens until the image changes. For the same reason, power consumption in this system depends on the amount of change in the visual image. For an unchanging image, very little power, attributable to bias currents and static leakage in digital circuits, is consumed. A second major challenge of this partition, which arises from the use of a digital bus to communicate between chips, is to avoid corrupting the low signal level analog signals used in the motion computation with noise from the digital portions of both chips.

In this work, we show that it is possible to efficiently split an STF-based motion computation into two modules without

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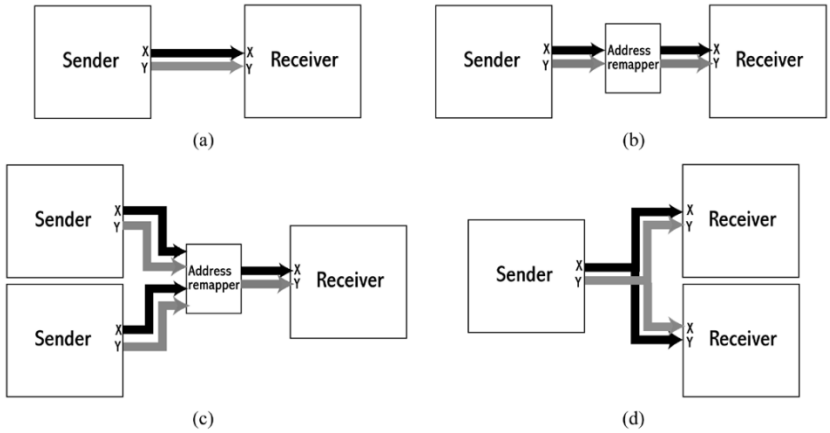

Fig. 1. A few of the many powerful vision system configurations using modular motion processing chips. **Sender** indicates a photosensitive sender chip with x and y address outputs shown. **Receiver** indicates a motion processing receiver with x and y address inputs shown. **Address remapper** indicates a static address remapping function. For simplicity, bus synchronization circuitry is not shown. (a) A single sender and receiver implement a 2-D array of one-dimensional (left-right) motion sensors with an output comparable to a monolithic implementation. However, the fill factor in this case is improved over a monolithic implementation. (b) Address remapping is performed between the sender and receiver chip. This might be, for example, a polar coordinate address remapping such that motion along the vertical axis of the receiver now corresponds to expansion in the visual image, and horizontal motion to rotation. In the same configuration, motion could be computed at a spatial frequency tuning lower than in panel **a** by mapping alternate rows and columns of the sender chip onto the receiver. (c) Outputs from two sender chips with convergent fields of view are interlaced onto the columns of a single receiver chip. Because the motion algorithm on the receiver chip expects the columns to be activated in sequence, this gives rise to a motion system with a preferred optical disparity. This system will respond to motion only at the depth at which the image is the same on both sender chips. (d) One sender coupled with two receivers can be used to compute two 2-D arrays of motion sensors. For example, the top receiver chip may compute the same motion outputs as in panel **a** (left-right). The bottom receiver chip receives exchanged x and y address buses, and thus computes a 90° rotated (up-down) and mirrored set of motion outputs. Similarly, using two receiver chips, motion could be simultaneously calculated at two different temporal frequency tunings.

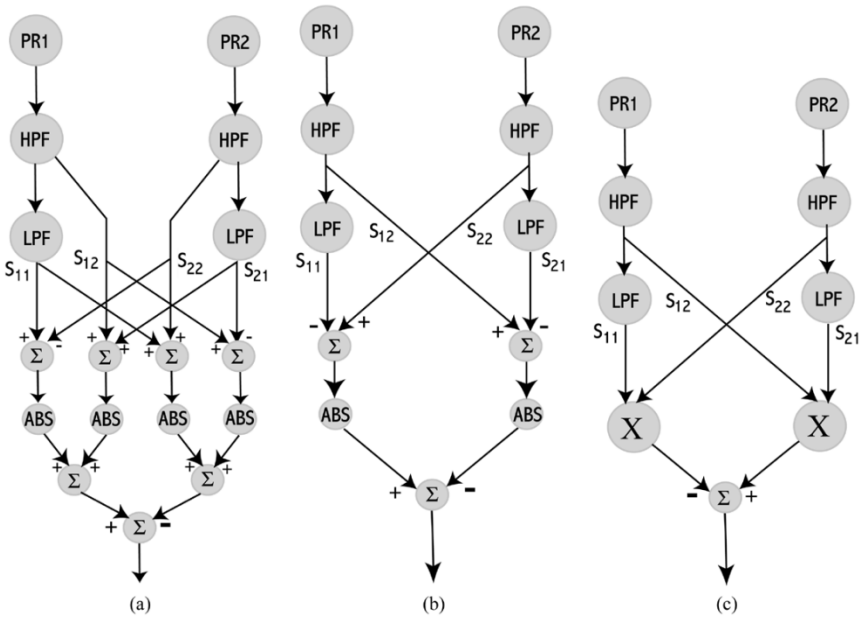

Fig. 2. Visual motion algorithms. (a) Adelson–Bergen (AB). (b) Barlow–Levick (BL). (c) Hassenstein–Reichardt (HR). HPF and LPF denote, respectively, high-pass and low-pass temporal filters. Σ indicates a summation. ABS denotes the absolute value operation, and $\mathbf{X}$ indicates multiplication. Each algorithm takes input from two neighboring visual sampling points, and provides an output the temporal mean of which indicates the direction of motion.

losing the advantages in power consumption and size over conventional approaches. We present implementations of three different STF-based motion algorithms and compare their performance, not only to each other but also to monolithic implementations of the same algorithms [16]. A novel element of our implementation is the use of a spike integrator to emulate the delay of a low-pass filter (LPF). We thus improve the fill factor while allowing significantly more complicated motion processing to be performed.

II. Visual Motion Algorithms

The three visual motion algorithms used in this paper (shown in Fig. 2) are the Adelson–Bergen (AB) motion energy model [19], the Hassenstein–Reichardt (HR) correlation model [20] and the Barlow–Levick (BL) motion detection model [21]. These algorithms were devised as biological models to describe, respectively, primate cortical complex cells, the opto-motor response in flies, and direction selectivity in the retina of

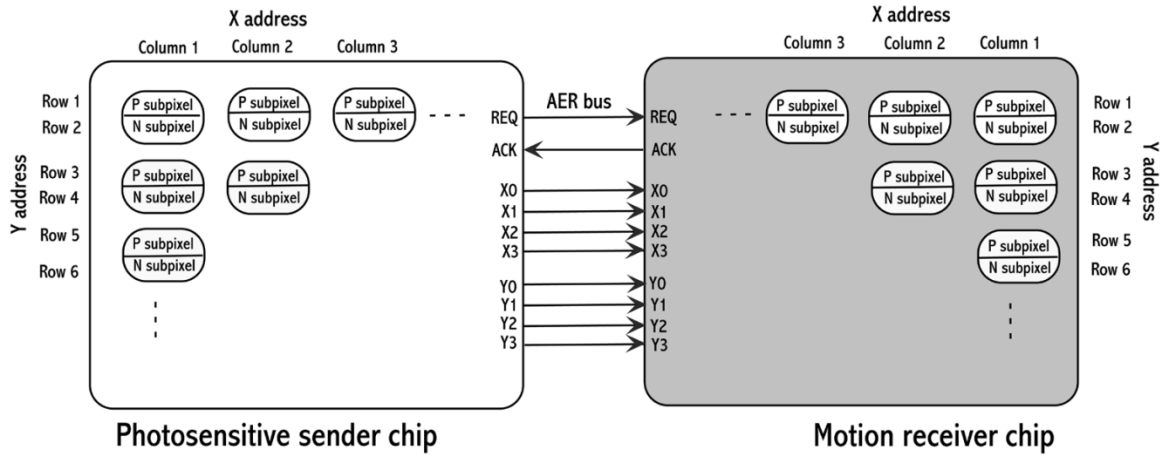

Fig. 3. The high-level architecture of a sender-receiver chip pair. Each pixel is composed of positive and negative sub-pixels that together process a complementary representation of intensity changes in the focal plane. P pixels on the sender chip transmit events indicating *increases* in local light intensity, while N pixels transmit *decreases*. Events arriving at P and N pixels on the receiver chip are integrated to compute the motion signal according to the specific algorithm. Results of the motion computation can be accessed via serial scanners.

a rabbit, and yet share many common features. They all remove the long-term illumination information using a high-pass filter (HPF), and compare the intensity from one visual sampling point with a delayed version (through an LPF) of a neighboring visual sampling point. Through different mathematical operations, all three algorithms represent in their mean output the energy in a band of spatial and temporal frequency which corresponds to motion. Each algorithm incorporates a nonlinearity, which is essential since all inputs to the motion detector (after high-pass filtering) are zero-mean, and the output of a linear system with these inputs must also have zero mean. Finally, all algorithms have been modified from their canonical form to facilitate circuit implementation. These algorithms are analyzed and compared mathematically in a related paper [16], which also describes and characterizes their monolithic analog VLSI implementations.

III. Multichip Implementation

To facilitate the kind of visual motion processing architectures shown in Fig. 1, we split the visual motion processing algorithms into two stages. The first stage, incorporating processing common to all three motion algorithms, contains a 2-D array of phototransduction circuits, and transmits information about local intensity changes across an asynchronous digital bus using the Address-Event Representation (AER) protocol, described below. The second stage, incorporating circuitry specific to the algorithm being implemented, contains circuitry to compute local visual motion. Since visual images change rather slowly, high-frequency responses of the analog circuitry are not required and thus subthreshold MOSFET biases are used wherever possible.

We have previously employed a similar multichip neuromorphic design strategy [17], [22], but the motion algorithm used in those cases was feature-based and did not operate at very low contrast. A number of other authors have published related designs, including Boahen [23] who computes visual motion with a photosensitive sender chip that is a model of the primate retina, and Indiveri *et al.* [24] who showed a multichip motion processor based on a silicon model of the primate visual cortex. See [22] for a review of modular multichip neuromorphic architectures.

The high-level architecture of the sender and receiver chips is illustrated in Fig. 3. The asynchronous digital bus between the two chips employs the AER protocol [18], [25], which multiplexes discrete "events" from every pixel on the sender chip onto a single bus with each event identified by its x and y spatial address. A four-phase handshake using request and acknowledge lines is used to communicate events between the two chips. Analogous to biological neurons encoding their activation in the frequency of action potentials, in our implementation the frequency of events transmitted from a particular spatial address on the sender chip represents the rate of intensity change at that location. Both sender and receiver chips are composed of a 2-D array of pixels, each of which consists of P and N sub-pixels. On the sender chip, the positive sub-pixel communicates intensity changes that increase from the mean luminance, and the negative sub-pixel communicates intensity decreases. The combination of these two channels accomplishes a *complementary coding* which allows the greatest precision when intensity changes are greatest. In the current implementation, the positive and negative sub-pixels share the same photoreceptor input. On the receiver chip, the two "spike trains" from the positive and negative pixel are integrated to compute local motion information. In each chip, analog and digital circuits are powered from separate supply lines to avoid noise coupling.

A. Photosensitive Sender Chip

The photosensitive sender chip consists of a 2-D focal plane array of pixels that are used to transduce and process local light intensity. Each pixel includes an adaptive photoreceptor [26], shown in Fig. 4(a), which adapts to the local light intensity on slow time scales providing high gain for transient signals that are centered on the adaptation point. This capability is utilized to extract intensity changes with respect to the adapted light level.

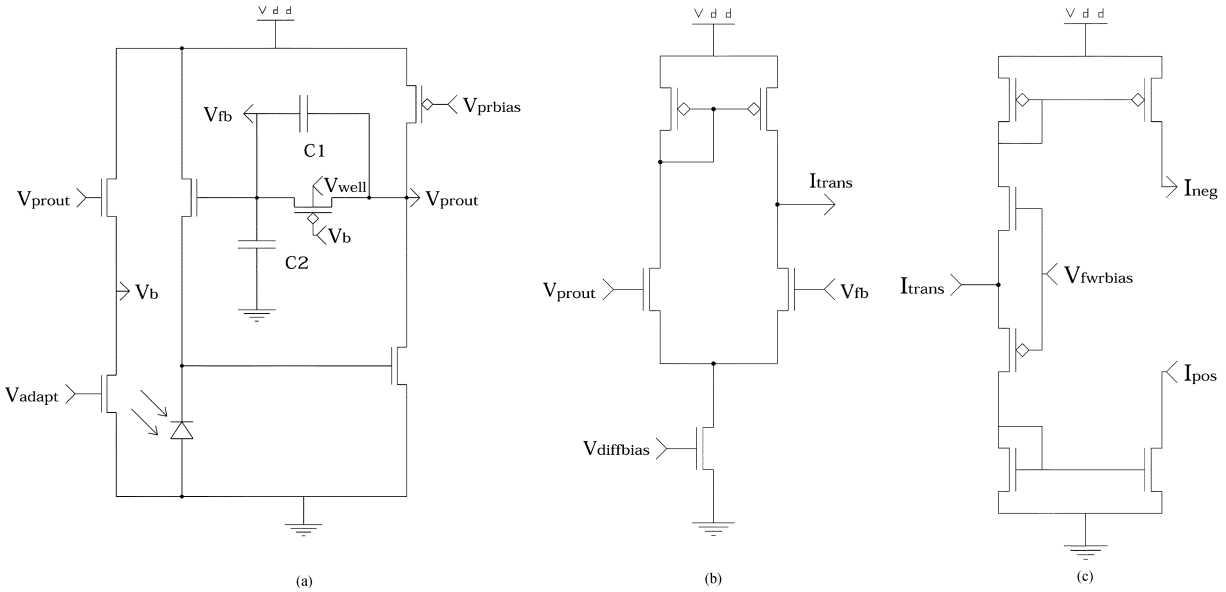

Fig. 4. Analog circuit building blocks used in the photosensitive sender pixel. (a) Adaptive photoreceptor [26]. This circuit provides an output $V_{\rm prout}$ sensitive to transient changes, and a long-term intensity output V_{fb}. $V_{\rm prbias}$ sets the frequency response and dc level of the output. $V_{\rm adapt}$ allows electronic adjustment of the adaptation time constant and is typically set at less than 300 mV for a time constant around 5 s. $V_{\rm well}$ is set near the dc level of $V_{\rm prout}$. (b) Simple transconductance amplifier circuit. $V_{\rm diffbias}$ controls the current output level. (c) Current-mode full-wave rectifier circuit [27]. $V_{\rm fwrbias}$ is set at a level favorable for the circuit providing $I_{\rm trans}$.

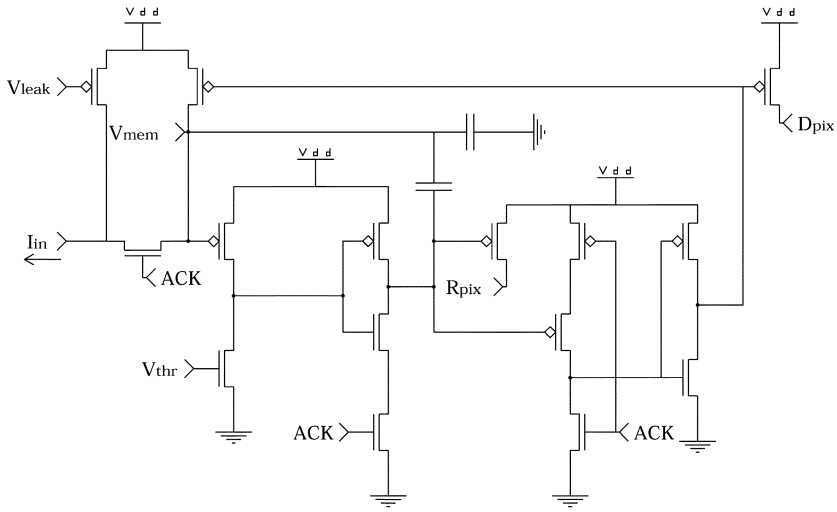

Fig. 5. AER sender pixel interface circuit, two of which are included in each sender pixel. This circuit communicates with peripheral sender circuitry to transmit local events off-chip. When the input current $I_{\rm in}$ exceeds the leak current controlled by $V_{\rm leak}$, it discharges the voltage $V_{\rm mem}$ until the threshold (set by $V_{\rm thr}$) of the double inverter is reached. The signal $R_{\rm pix}$ is then asserted to the row arbiter. When acknowledged by the signal ACK, the vertical signal $D_{\rm pix}$ is sent to a column latch, which also resets $V_{\rm mem}$.

The capacitor ratio C_2/C_1, to which the transient gain is proportional, is 11. The photoreceptor output $V_{\rm prout}$ is used in conjunction with the voltage V_{fb} that represents the adaptation state of the photoreceptor in order to remove the mean light intensity from the input signal, accomplishing the high-pass filtering step common to all motion algorithms. A simple transconductance amplifier [Fig. 4(b)] is used to convert the difference of these two voltages into a current, which is then separated into its positive and negative components using a full-wave rectifier circuit [27] [Fig. 4(c)]. The resulting currents $I_{\rm pos}$ and $I_{\rm neg}$ correspond, respectively, to increases and decreases in local luminance.

These two currents are then fed into two separate AER interface circuits, shown in Fig. 5. The negative current must be mirrored before being connected to this circuit. In each case, a bias current (from the $V_{\rm leak}$ transistor) is provided to prevent AER bus response to noise. These circuits generate 2-D requests to the peripheral AER interface circuitry, such that trains of events representing the value of the two currents $I_{\rm pos}$ and $I_{\rm neg}$ are transmitted to the receiver chip. Positive and negative events from the same pixel share a common column address, but are in neighboring rows in the AER address space.

The details of the AER interface circuit are explained in [28], and the peripheral AER circuitry in [18]. The sender chip also contains serial scanners [29] to allow for readout of the raw photoreceptor values. A summary of the specifications of the sender chip is given in Table I.

TABLE I
MODULAR MOTION SENDER/RECEIVER CHIP SPECIFICATIONS. EACH CHIP WAS FABRICATED IN A 1.6-μm PROCESS ON A 4.41-mm^2 DIE. SENDER CHIP PIXEL ALSO CONTAINS A 1378-μm^2 PHOTODIODE, YIELDING A FILL FACTOR OF 4.8%. NOTE THAT A LARGE PERCENTAGE OF EACH RECEIVER PIXEL IS DEVOTED TO SPIKE INTEGRATION CAPACITORS

Sensor	Array Size (pixels)	Pixel transistor count	Pixel capacitor count	Pixel area (μm^2)	Percent pixel area capacitance
Sender	6 × 6	49	6	28452	4.4
AB receiver	6 × 6	57	4	45841	38.5
BL receiver	6 × 7	39	4	38081	47.3
HR receiver	6 × 7	65	4	38081	34.4

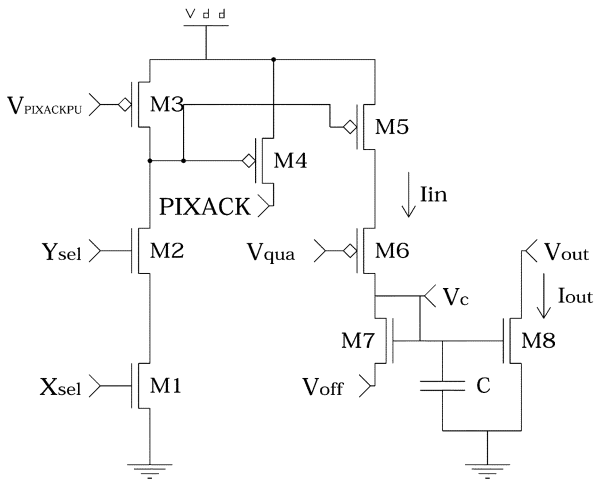

Fig. 6. AER receiver pixel interface circuit. This circuit receives decoded labeled-line requests from the peripheral circuitry on signals $X_{\rm sel}$ and $Y_{\rm sel}$ and acknowledges the event with signal PIXACK while integrating the received spike on the capacitor C. Bias $V_{\rm pixackpu}$ prevents charge pumping. Parameters of integration are controlled by biases $V_{\rm qua}$ and $V_{\rm off}$ (see text).

B. Motion Computing Receiver Chips

The motion computing receiver chips are designed to perform small field motion computation by processing the intensity change information transmitted by the photosensitive sender chip. These receiver chips have the same high-level chip architecture but realize different STF tuned motion computation models. Every receiver chip is composed of peripheral AER interface circuitry, a 2-D array of motion computation pixels each of which incorporates an AER pixel interface circuit, and serial scanners [29] to allow readout of the motion response of each pixel.

Peripheral address decoding and interface circuitry to support the protocol are discussed in detail in [18]. The AER pixel interface circuit in the receiver chip is illustrated in Fig. 6. Intensity changes in the focal plane of the sender chip result in events being transmitted on the AER bus to the receiver chip. The interchip request signal with its two-dimensional address activates the corresponding pixel in the receiver. This is achieved by using address decoders to activate a particular pixel's $X_{\rm sel}$ and $Y_{\rm sel}$ signals, which pulls low the gate of transistor M5, creating an input voltage "spike". The receiver pixel acknowledges the signals sent by the peripheral AER circuitry by pulling high the *PIXACK* signal, which results in the release of the pixel selection signals, ending the input voltage spike. A sequence of these spikes is integrated onto the capacitor resulting in an output current $I_{\rm out}$, which is used in the motion computation.

In this work, we utilize the spike integrator circuit not only to convert the incoming spikes back into an analog signal but also to obtain the required delay, shown in Fig. 2 as an LPF, between neighboring pixel signals. In order to justify that such an implementation is reasonable, the output current of the circuit is formulated below in terms of bias voltages and the frequency of spikes coming into a particular pixel. Afterwards, the details of each algorithm's implementation are described.

1) Variable Phase Delay Using Spike Integrators: Referring to Fig. 6, we formulate the input current $I_{\rm in}$ in terms of the incoming spike train. For the purposes of this derivation, we assume that MOSFETs operate in the subthreshold regime. Let the spike frequency f be a function of time, but assume for simplicity that the input spike frequency is significantly higher than the rate of change of the spike frequency. For each pulse of stereotyped width T, a quantum of charge is delivered which is closely approximated by

$$Q = T \cdot I_0 e^{\kappa(V_{dd} - V_{\rm qua})} \tag{1}$$

where V_{dd} is the power-supply voltage, I_0 is the preconstant for subthreshold PFET current, and κ is the parameter which relates changes in gate voltage to changes in channel surface potential. At the given spike rate, an average input current is delivered of

$$I_{\rm in} = f \cdot Q = f \cdot T \cdot I_0 e^{\kappa(V_{dd} - V_{\rm qua})}. \tag{2}$$

Given a particular input current, the current integrator circuit can be shown to act as a linear first-order LPF in the special case where variations in $I_{\rm out}$ are small relative to the sustained value of $I_{\rm out}$. This corresponds to the assumption about spike frequency made above.

We start the analysis of the circuit by writing a KCL equation at the capacitor node

$$I_{\rm in} = I_{M7} + I_C. \tag{3}$$

The capacitor current can be written as $I_C = C(\delta V_C/\delta t)$. Since the output current $I_{\rm out}$ is amplified by the current mirror tilt $V_{\rm off}$, the output current can be formulated in terms of I_{M7} and $V_{\rm off}$ as $I_{\rm out} = I_{M7} e^{(V_{\rm off}/V_T)}$. In order to represent $I_{\rm out}$ in terms of $I_{\rm in}$, we use the chain rule to relate the time derivative of $I_{\rm out}$ to the time derivative of V_C

$$\frac{\delta I_{\rm out}}{\delta t} = \frac{\delta I_{\rm out}}{\delta V_C}\frac{\delta V_C}{\delta t} \tag{4}$$

where

$$\frac{\delta I_{\rm out}}{\delta V_C} = \frac{\kappa I_{\rm out}}{V_T} \tag{5}$$

and since $(\delta V_C/\delta t) = (I_C/C)$ and $I_C = I_{\rm in} - I_{M7}$, we can obtain the following equation:

$$\frac{\delta V_c}{\delta t} = \frac{1}{C}\left(I_{\rm in} - I_{\rm out} e^{-\frac{V_{\rm off}}{V_T}}\right). \tag{6}$$

By combining (4), (5), and (6), we can show that the relation between $I_{\rm out}$ and $I_{\rm in}$ can be expressed as follows:

$$\frac{\delta I_{\rm out}}{\delta t} = \frac{\kappa I_{\rm out}}{C V_T}\left(I_{\rm in} - I_{\rm out} e^{-\frac{V_{\rm off}}{V_T}}\right) \tag{7}$$

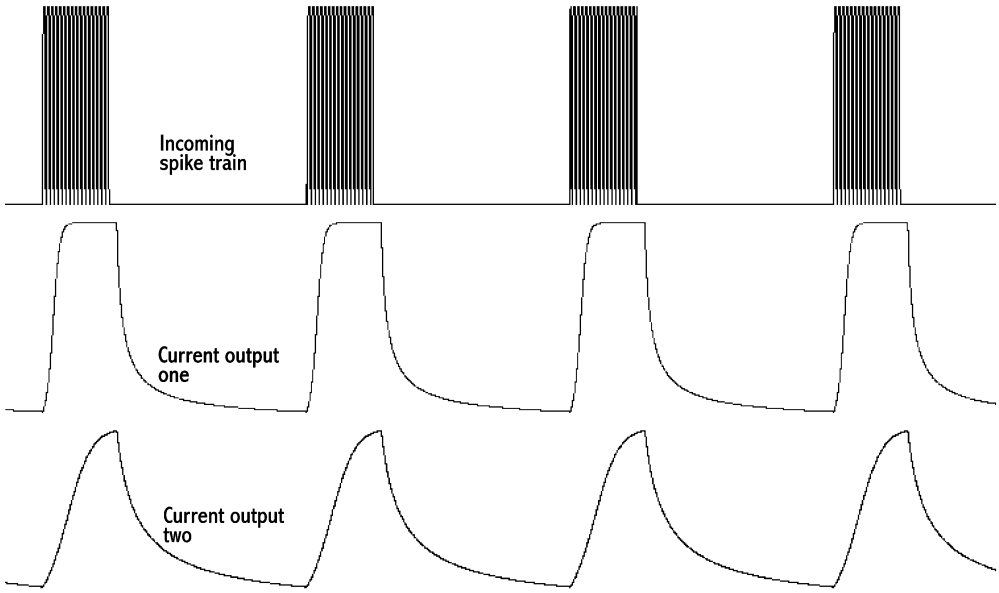

Fig. 7. Simulated current outputs of two integrators biased with different $V_{\rm qua}$ and $V_{\rm off}$ biases. A periodic spike train is provided to the two integrators. The first integrator is biased with a stronger $V_{\rm qua}$ than the second. To compensate for the resulting difference in the amplitude of these currents, $V_{\rm off}$ is biased more strongly for the second integrator than the first. These biases yield a relatively slower current response from the second integrator with approximately the same magnitude.

or further, as

$$\tau \frac{\delta I_{\rm out}}{\delta t} = I_{\rm in} e^{\frac{V_{\rm off}}{V_T}} - I_{\rm out} \tag{8}$$

where $\tau = (CV_T/\kappa I_{\rm out}) e^{(V_{\rm off}/V_T)}$. If $I_{\rm out}$ can be considered constant (relative to its changes), we can take the Laplace transform to obtain

$$\frac{I_{\rm out}}{I_{\rm in}} = \frac{e^{\frac{V_{\rm off}}{V_T}}}{1+\tau s}. \tag{9}$$

This equation shows that the current-mode integrator can be used as a first-order LPF in the special case where the input spike frequency is significantly higher than the rate of change of the spike frequency. The $V_{\rm off}$ bias voltage provides current gain at the output node to set the desired level. The time constant τ can be reformulated in terms of the input current by realizing that, on long time scales, $I_{\rm out} = I_{\rm in} e^{V_{\rm off}/V_T}$. Thus

$$\tau = \frac{CV_T}{\kappa \cdot f \cdot T \cdot I_0 e^{\kappa(V_{dd} - V_{\rm qua})}} \tag{10}$$

where the terms involving $V_{\rm off}$ divide out. The bias voltage $V_{\rm qua}$ controls the time constant of the filter. This circuit is ideal for providing a phase delay, because the signal attenuation encountered when using a LPF for phase delay can be compensated for using the $V_{\rm off}$ gain term.

Even in the case where our assumption of a high input spike frequency relative to changes in the spike frequency is violated, the integrator circuit can be used to provide delay [30], although it is not equivalent to a linear filter. Fig. 7 illustrates such a case in which the output of two integrator circuits operating on the same input spike train are biased to have different phase delays.

2) AB Sensor: The AB motion energy model was explicitly formulated to extract the energy in a band of spatial and temporal frequency. In its canonical form, it obtains its direction selectivity by integrating quadrature filters with a nonlinear squaring function. A version of the AB algorithm was implemented on a general-purpose analog neural computer by Etienne-Cummings *et al.* [12]. Later, Higgins and Korrapati [16], [31] implemented a monolithic analog VLSI sensor based on this algorithm.

In the present implementation, the algorithm for which is shown in Fig. 2(a), the spatial filtering is trivialized by simply using two neighboring photoreceptor outputs. This provides the necessary spatial phase difference between the two photoreceptor inputs, but does not achieve quadrature phase. Spike integration circuits were used to emulate temporal filters in the model. Since spike integration circuits are a necessary part of the AER communications system, this is highly parsimonious. Each incoming spike train is integrated simultaneously by two spike integrator circuits adjusted to have different phase delays by using their respective biases $V_{\rm qua1}$ and $V_{\rm qua2}$. Thus, one channel is delayed relative to the other. This requires duplication only of transistors M6 through M8 from Fig. 6; transistors M1 through M5 are shared between the two spike integrators. Additionally, since each output current is needed in two places to complete the local motion computation, and again in two places in the neighboring motion computation, transistor M8 is replicated four times in each spike integrator. Finally, the nonlinearity required to realize the algorithm is attained in the implementation by employing an absolute value operation.

The multichip implementation of the AB algorithm is illustrated in Fig. 8(a). On the sender chip, each photoreceptor's response is split into two channels corresponding to increasing and decreasing intensity from the long-term mean. On the receiver chip, each of these channels is converted to a current with a pair of integrator circuits, one of which is delayed relative to the other. The remainder of the computation is performed in current mode, largely by utilizing Kirchoff's current law to perform

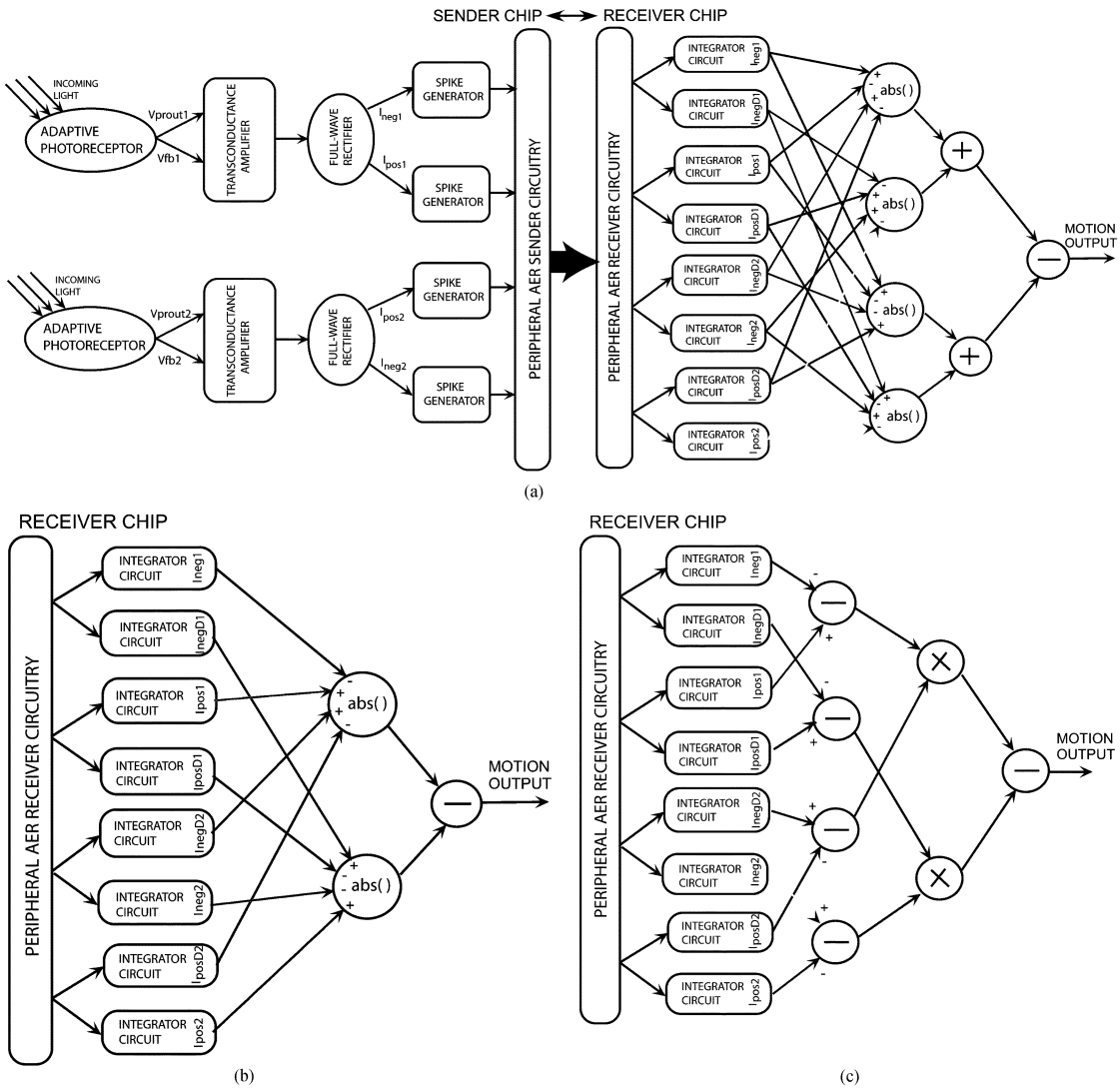

Fig. 8. Block diagrams of multichip motion sensor implementation. (a) Adelson–Bergen. (b) Barlow–Levick. (c) Hassenstein–Reichardt. For the BL and HR implementations, only the receiver portion is shown; the sender portion is identical in all three implementations. $V_{\rm prout}$ and V_{fb} represent the photoreceptor transient and sustained illumination output, respectively. In the sender portion, $I_{\rm pos}$ and $I_{\rm neg}$ refer to positive and negative parts of the photoreceptor signal, and in the receiver portion, $I_{\rm pos}$ and $I_{\rm neg}$ represent the integrated versions of these signals. $I_{\rm pos}D$ and $I_{\rm neg}D$ are the signals that are delayed relative to $I_{\rm pos}$ and $I_{\rm neg}$.

sums. Current mirrors are used to reverse the sign of current signals. A current-mode absolute value circuit [32], [Fig. 9(a)] is used to implement the necessary nonlinearity. The bias $V_{\rm casp}$ is set close enough to V_{dd} that when the PFET current mirror is conducting, the drain of the input transistor cuts off current flow through $M_{\rm casp}$ (and thus the NFET mirror). Conversely, when the PFET mirror is turned off by current flow in the opposite direction, $M_{\rm casp}$ is turned on to allow current flow through the NFET mirror. By setting $V_{\rm casp}$ very high, it is possible to limit the current through the NFET mirror and thus control the relative contribution of positive and negative currents to the absolute value. Each pixel in the AB receiver chip consists of two spike receiver circuits (each with a pair of accompanying integrators), four absolute value circuits, and 5 current mirrors. A summary of the specifications of the AB receiver chip is given in Table I. Much of the pixel area is used for conservatively large spike integration capacitors, which for the two spike integrators in each sub-pixel are approximately 5 and 7 pF. Since one of the spike integration capacitors is larger than the other, there is still a relative delay even at the same $V_{\rm qua}$ bias setting.

3) BL Sensor: The BL motion detection model [21] uses a local photoreceptor signal with an inhibitory connection from a neighboring photoreceptor to obtain direction selectivity. Benson and Delbruck [33] utilized a similar inhibition mechanism to implement a monolithic analog VLSI vision sensor.

The version of the BL algorithm implemented in this work is shown in Fig. 2(b). Similar to the AB implementation described above, the BL implementation uses spike integrators to achieve the necessary delay between incoming spike trains. Each spike integrator current is needed only once to complete the local motion computation, and once again in the neighboring motion computation, so transistor M8 in Fig. 6 is replicated only twice in each spike integrator. The receiver chip computation is illustrated in Fig. 8(b). Following the integrator outputs, three current mirrors and two current-mode absolute value circuits [Fig. 9(a)] are necessary to complete the computation.

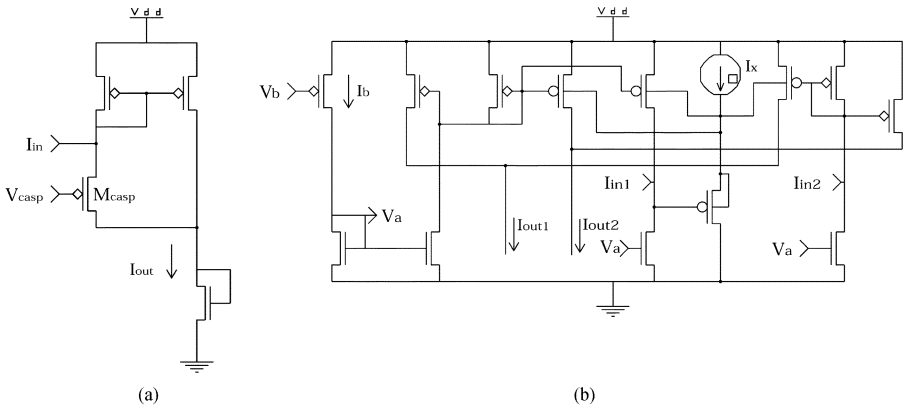

Fig. 9. Analog circuit building blocks used in the motion computing receiver pixels. (a) Absolute value circuit [32]. Regardless of its sign, the input current is gated to $I_{\rm out}$. $V_{\rm casp}$ can be used to control the relative contribution of positive and negative currents to the output. (b) Four quadrant current multiplier [38]. V_b and I_x provide bias currents. $I_{\rm in1}$ and $I_{\rm in2}$ are the bidirectional input currents, and $I_{\rm out1}$ and $I_{\rm out2}$ are the output currents, meant to be sensed at low output voltages. The difference of output currents gives the final output $I_{\rm out} = (I_{\rm in1}I_{\rm in2})/(I_b)$ for $|I_{\rm in1}|$ and $|I_{\rm in2}| > I_b$.

A summary of the specifications of the BL receiver chip is given in Table I. In comparison to the HR and AB implementations, this motion detection pixel contains significantly fewer transistors. Nearly half of the layout for this receiver pixel was used for large spike integration capacitors.

4) HR Sensor: The HR correlation model is similar to the BL model described above, but employs a multiplication for the interaction of its delayed and undelayed input channels. This model was originally proposed to explain the optomotor response of the beetle *Chlorophanus* [20]. In a variety of studies the HR correlation model has been implemented on monolithic analog VLSI chips to estimate the local motion field [13], [34]–[36]. Most closely related to this work, Liu [36] and Harrison [13] have used this algorithm to model the fly's motion detection system.

The version of the HR algorithm implemented in this work is shown in Fig. 2(c). Similar to both implementations previously described, the HR implementation uses integrators to provide the necessary delay between photoreceptor channels. Like the BL implementation, each spike integrator current is needed only once to complete the local motion computation, and once again in the neighboring motion computation, so transistor M8 in Fig. 6 is replicated only twice in each spike integrator. The receiver chip computation is illustrated in Fig. 8(c). Five current mirrors are necessary to accomplish the subtractions, and two four-quadrant current-mode multipliers (shown in Fig. 9(b)) are used. A summary of the specifications of the HR receiver chip is given in Table I.

IV. Characterization Results

In this section, we present detailed characterization results of three motion processing systems, each consisting of the photosensitive sender chip paired with one of the three motion receiver chips described in the previous section. The characterizations were performed by presenting the sender chip with computer-generated 2-D sinusoidal grating stimuli on an LCD screen (see [16] for more details of our characterization methods). The current output of a single pixel of each sensor was converted to voltage by utilizing an off-chip current sense amplifier. Raw outputs were averaged over ten temporal periods of the stimulus to remove the phase dependence of the sensors.

We refer to stimuli which move in that direction which elicits the largest positive mean current output from the sensor as *preferred direction stimuli*, and stimuli which move in that direction which elicits the largest negative mean current output from the sensor as *null direction stimuli*. Each chip was biased to maximize the difference between mean outputs in response to preferred and null direction stimuli (which we use as a definition of good performance) at an output current in the nanoamperes. At a given bias setting, we define the "optimal" stimulus (or stimulus parameter value) as the one that maximizes the difference between mean outputs to preferred and null direction stimuli. Whenever one or more parameters were being varied, all other parameters were held at their optimal value. Each chip was characterized with the same fixed mean illumination. The optimal value of spatial frequency was 0.25 cycles per chip pixel. Each chip was tuned for an optimal temporal frequency of 3 Hz.

The first visual characterization experiment was performed by using a sinusoidal grating stimulus to test the direction selectivity of the sensors for motion in the preferred direction (which elicits a positive mean output from the sensor), for motion orthogonal to the sensor orientation (which elicits a zero mean output), motion in the null direction (eliciting a negative mean output), and for a nonmoving grating (which results in zero output). The results of this experiment are seen in Fig. 10, and quite clearly show their direction selectivity, as well as the waveshape of the response of each sensor.

In Fig. 11, the spatiotemporal response of the sensors are shown. These plots show the mean output of each sensor to sinusoidal stimuli over a range of spatial and temporal frequency. The sensors respond best to a particular combination of spatial and temporal frequency for which they are tuned and responses decrease at other frequencies. The optimal temporal frequency can be tuned electronically by altering the value of the integrating receiver circuit bias voltages $V_{\rm qua1}$ and $V_{\rm qua2}$ as illustrated in Fig. 12.

Next, stimulus contrast was varied over the entire range possible with the LCD screen used in the experiment. Fig. 13 shows the mean output of each sensor as contrast is changed. All the

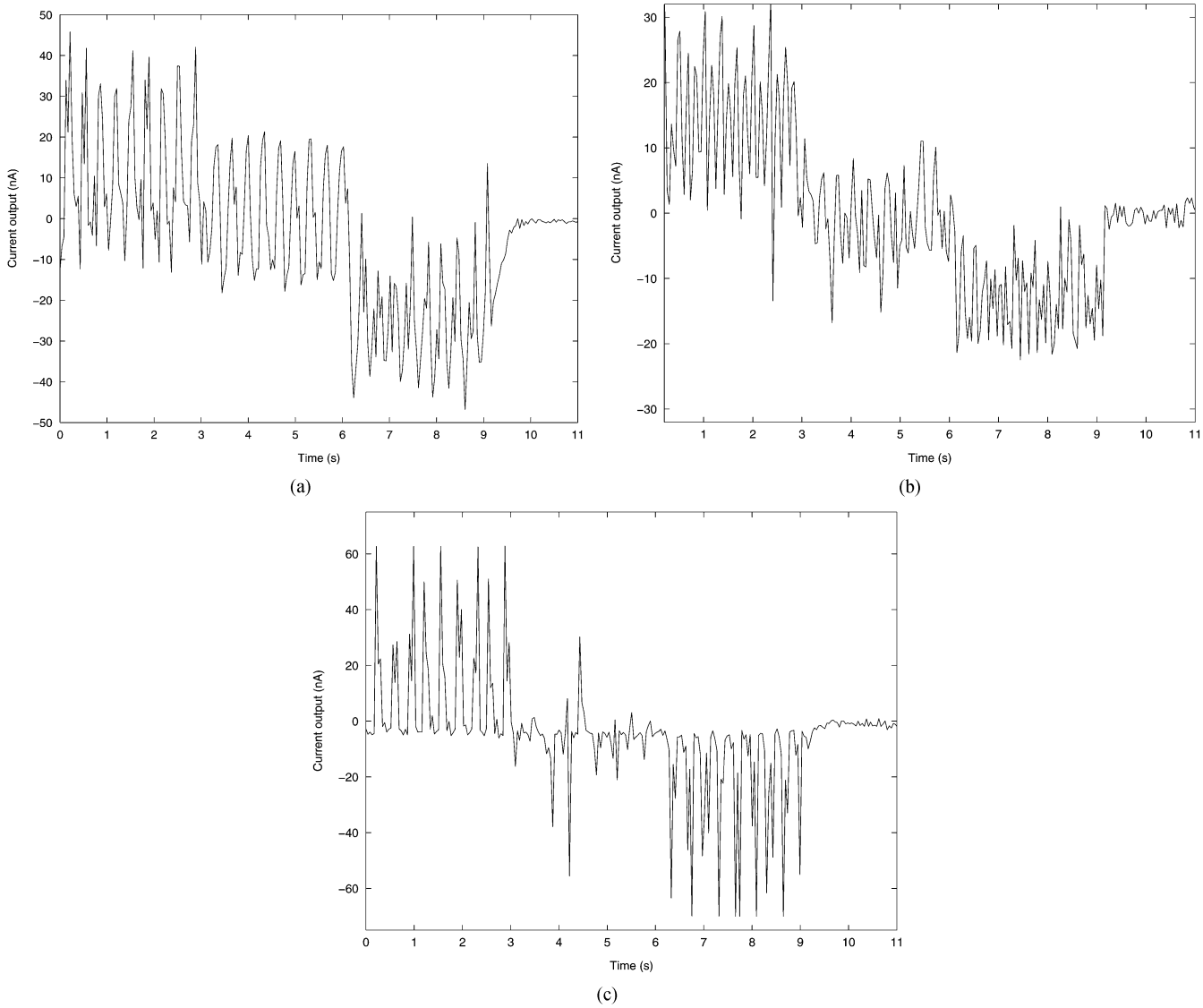

Fig. 10. Raw temporal output of the motion sensors (in nanoamperes). (a) AB sensor. (b) BL sensor. (c) HR sensor. These outputs are not averaged and represent the real time single pixel response of the sensors. In the interval from 0 to 3 s a sinusoidal stimulus is presented in the preferred direction (positive mean output). Between 3 and 6 s a stimulus moving orthogonal to the sensor orientation is presented (zero mean output). Between 6 and 9 s, the sensor is exposed to a null direction stimulus (negative mean output). Finally, a stationary stimulus is presented between 9 and 11 s.

sensors responded strongly down to 10% contrast and determination of the direction of motion was possible at significantly lower contrasts. The HR sensor's mean output is negative to preferred-direction stimuli at low contrast (see Discussion).

Since the power consumption of each chip in this system is data dependent, power-supply current for each chip was measured both while unstimulated, and during operation with an optimal sinusoidal visual stimulus. Note that biases were optimized for performance, not for low power consumption. Power consumption figures are summarized in Table II.

V. Discussion

We have presented a modular multichip implementation of visual motion algorithms which makes possible the efficient board-level implementation of complex visual motion processing schemes. The results shown demonstrate that we have been able to overcome the noise difficulties of mixed-signal VLSI design to achieve performance comparable to monolithic implementations of the same algorithms [16]. The presented designs all have a saturating response to the contrast of moving stimuli, are capable of the detection of visual motion with as little as a few percent contrast, and are tunable to motion at temporal frequencies as low as 0.2 Hz.

Since this system fundamentally performs a low signal-level analog motion computation, but also incorporates high signal-level asynchronous digital circuitry, a number of mixed-signal design features were required to avoid the undesired introduction of noise onto the analog signals. On all chips, separate power-supply lines are provided for analog (relatively steady power consumption) and digital (switching power consumption) signals to avoid noise coupling through the power supply. These power supplies are separately regulated off-chip. Most circuits are designed using a differential current signal representation to reduce capacitively coupled noise. Large spike integration capacitors are used to reduce the impact of the AER bus spike

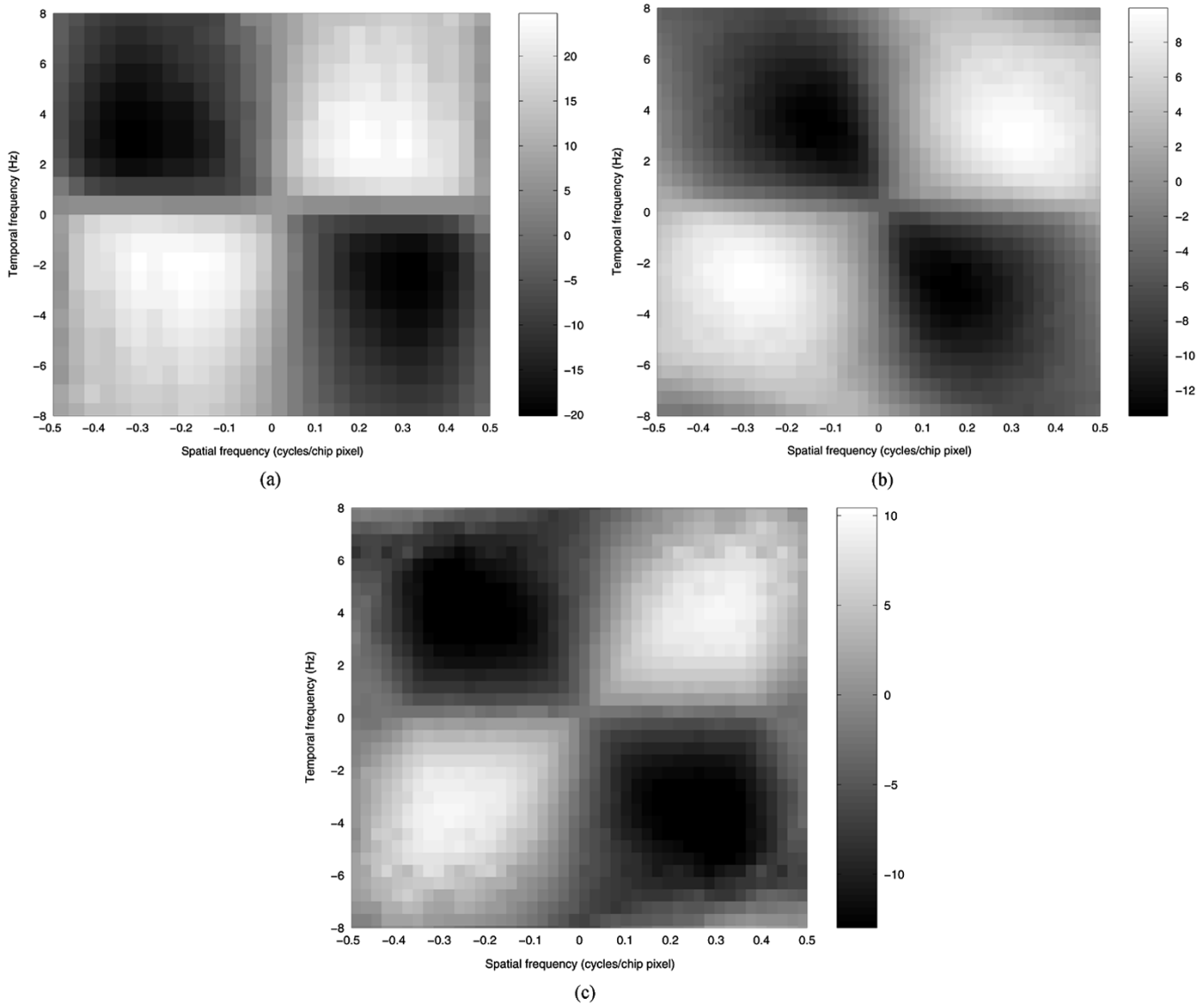

Fig. 11. Mean output of the motion sensors to variation of spatial and temporal frequency, shown in nanoamperes. (a) AB sensor. (b) BL sensor. (c) HR sensor. Each point on these plots indicates the mean output of a sensor to a sinusoidal stimulus with a particular combination of spatial and temporal frequency. Lighter gray levels indicate positive and darker gray levels indicate negative mean output.

rate on the analog signals in the receiver chip. In all pixel designs, analog circuitry is isolated from the substrate minority carrier injection of digital circuitry at the layout level by the use of guard structures. Additionally, the core of each chip (incorporating all of the analog circuitry) is isolated from the asynchronous digital periphery by a large guard ring.

The multichip implementation of the AB algorithm is quite similar to its monolithic implementation, while the two implementations of the BL and HR algorithms have considerable differences. These differences are driven by the fact that, in the multichip implementation, all photoreceptor signals arrive for motion processing in current mode. All monolithic implementations use a voltage-mode g_m-C LPF to produce the required delay, while the multichip implementations use the AER spike integration circuits for this purpose. After delay filtering, the AB receiver chip employs the same current-mode circuitry as in the monolithic implementation. Unlike the monolithic BL implementation, the BL receiver chip performs signal differencing in current mode and employs a simpler absolute value circuit. The HR receiver chip multiplies signals in current-mode, whereas the monolithic HR implementation uses a voltage-mode Gilbert multiplier. By limiting the photoreceptor signal processing circuitry in the focal plane, the sender chip achieves a fill factor of approximately 5%, which is better than two out of the three monolithic implementations, while allowing for much more complex motion computations than the monolithic implementations.

The raw data of Fig. 10 show the direction selectivity of each sensor. Note that, despite the mixed-signal nature of this design, these analog signals are not overly corrupted by noise at the relatively high frequency of the digital interchip communications bus. The fact that asynchronous data transmission is used to produce the data is apparent in the HR raw output for orthogonal stimuli, which relies on a precise balance between signals from neighboring photoreceptors. This HR output shows spikes of both signs at random, due to minor signal variations from

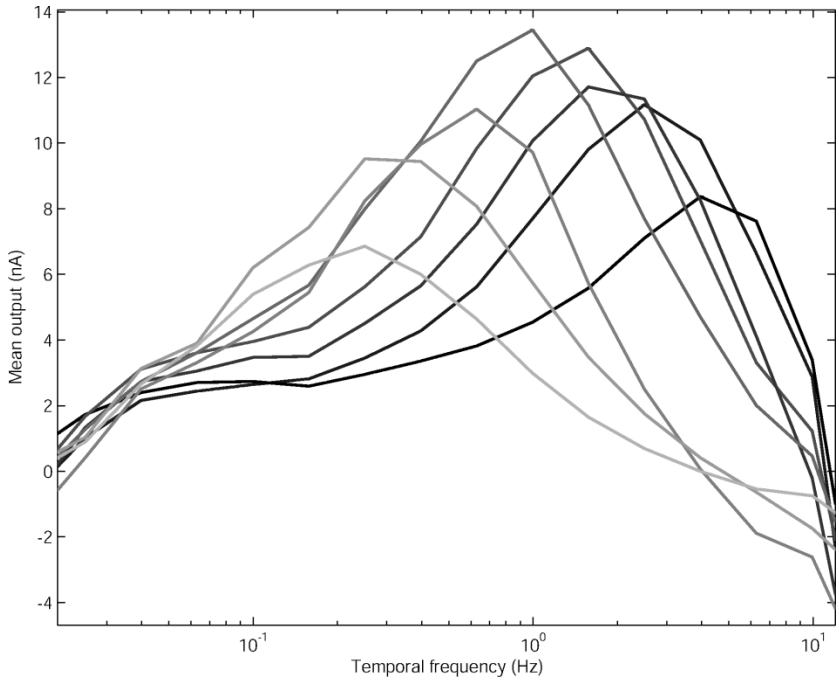

Fig. 12. Variation of temporal frequency tuning, illustrated for the BL sensor. By changing the spike integrator biases V_{qua1} and V_{qua2}, it is possible to change the temporal frequency tuning of the sensor. For this experiment, V_{qua1} was fixed at 4.12 V. Each curve in these plots is at a different V_{qua2} bias setting, varying from 4.19 V (lowest center frequency) to 3.93 V (highest center frequency). Each curve shows the mean sensor output in response to a sinusoidal stimulus in the preferred direction as temporal frequency is varied. The overall envelope of all plots is the photoreceptor temporal frequency response, the low frequency cutoff of which is due to adaptation, and the high frequency cutoff of which is due to the capacitance driven at its output and its bias setting.

the sender chip. Each algorithm is clearly able to represent the direction of motion in its mean output and, allowing for differences in implementation, the waveforms are qualitatively comparable to those of the monolithic implementations of the same algorithms.

The STF plots for each sensor (Fig. 11) show a tuning in both spatial and temporal frequency, as observed in the monolithic implementations and predicted by theoretical analysis [16]. Each sensor shows a peak response at a spatial frequency of approximately 0.25 cycles per pixel, as expected from the theoretical analysis. The AB and BL sensors show a slight offset in spatial and temporal frequency between the positive and negative peak responses. This is due to minor differences between the delays in the two "low-pass filtered" pathways of the motion detector, likely caused by mismatch in the spike integrator circuits. Fig. 12 shows that, by alteration of the V_{qua} biases, the peak temporal response frequency of the sensors can be adjusted over a wide range, limited by the photoreceptor bandpass frequency response. At a single bias setting, the sensors can detect motion for a speed range of more than one order of magnitude. These responses justify the use of the spike integration circuit as a temporal filter in the motion computation.

The responses to contrast shown in Fig. 13 saturate, such that for contrasts greater than 20% all stimuli elicit nearly the same mean output. This saturation arises from the sender chip, and is due to current output saturation of the transconductance amplifier used to remove the mean luminance from the photoreceptor signal. This rejection of contrast is a highly desirable quality, allowing response to motion without undue regard to contrast, and is also observed in biological motion-sensitive cells [37], and in the monolithic implementation of the AB sensor.

The contrast data for the HR sensor [Fig. 13(c)] show an interesting artifact in which mean outputs at very low contrast are all negative. This arises from our use of the four quadrant multiplication circuit [Fig. 9(b)] in the HR receiver pixel. Due to the Early effect, this circuit works precisely as a four quadrant multiplier only if the output currents I_{out1} and I_{out2} are held at the same voltage. Diode-connected transistors are meant to be used here to mirror out each current, but in our implementation we used a current mirror to directly subtract these two current outputs to save transistors. Due to this shortcut, at low current levels the mismatch due to the Early effect leads to an undesired change of sign.

Power consumption figures are summarized in Table II. The power consumption of the presented designs (roughly 10 mW for any sender/receiver pair) is considerably above that of the monolithic versions (which all consumed whole-chip power in the hundreds of microwatts), primarily due to power consumption by digital bias structures. This power consumption results from passive pull-up and pull-down transistors in the peripheral AER circuitry, most of which scale with the number of rows and columns of the processor array. The analog circuits in the processor array consume a modest amount of power, which is mostly consumed in bias currents and thus independent of visual stimulation. When stimulated, the AER communications circuitry consumes additional power ("Added DVdd" column) to transmit data from sender to receiver. All four of the the presented designs were fabricated on minimum-size dies in a low-cost experimental process available through MOSIS, and thus the pixel counts are extremely small by modern standards.

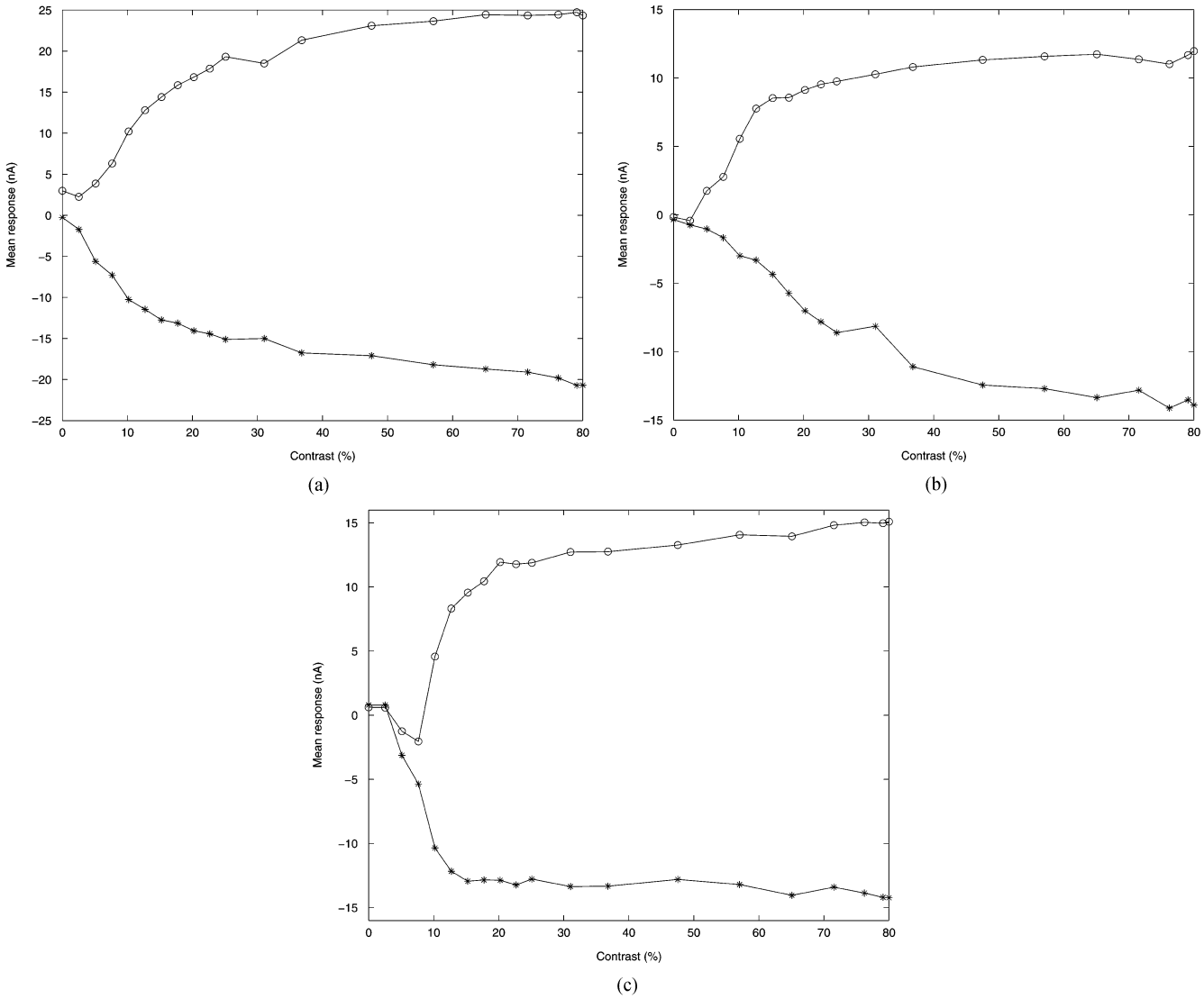

Fig. 13. Variation of the contrast of a sinusoidal stimulus. The responses represent the mean output of the sensors in nanoamperes. Circles indicate motion in the preferred direction; asterisks in the null direction. (a) AB sensor. (b) BL sensor. (c) HR sensor. While all sensors share a saturating response to contrast and all sensors are able to determine stimulus direction at less than 10% contrast, they do differ in the details of their low contrast response. The HR sensor, in particular, has a negative mean output to low contrast stimuli of either direction (see text). Due to the brightness of the "black" regions of the LCD screen, the maximum possible contrast was approximately 80%.

However, due to the pixel-parallel nature of the design, there is no technical obstacle to the fabrication of larger arrays. As a first order approximation, as each array is scaled up the digital bias power scales with the number of rows/columns, the analog bias power scales with the pixel count, and the communications power scales as the logarithm of the number of rows/columns (that is, the size of the interchip communications bus). By this method, the total power consumption (at the same bias settings) of a practically realistic 64×64 sender/receiver pair would be 183 mW. However, the same size monolithic motion processor array (using the lowest monolithic pixel power consumption of 1.04 μW/pixel) would only consume 4.3 mW (around 43 times less power). Even taking the array size to an extreme 300×300, the power consumed by the multichip system (2.6 W) is 28 times more than the comparable monolithic system (94 mW). Though at any reasonable resolution the multichip implementation does not approach the power consumption of a monolithic design, the power figures are still likely below those of an embedded CCD/DSP combination performing the same task in real-time.

TABLE II
BEST-PERFORMANCE TOTAL POWER CONSUMPTION OF MODULAR MOTION CHIPS. DVdd COLUMN INDICATES POWER SUPPLIED TO DIGITAL CIRCUITS; AVdd COLUMN INDICATES POWER SUPPLIED TO ANALOG CIRCUITS. TOTAL POWER FIGURES LISTED ARE FOR ENTIRE CHIP INCLUDING BOTH ANALOG AND DIGITAL POWER SUPPLIES. THE 'ADDED DVdd' COLUMN INDICATES THE INCREASE IN DVdd POWER CONSUMPTION DUE TO AER BUS RESPONSE TO VISUAL STIMULATION; AVdd POWER CONSUMPTION HAD NO MEASURABLE STIMULUS DEPENDENCE. IN ALL CASES, POWER-SUPPLY VOLTAGE WAS 5 V

VLSI chip	**Unstimulated power** (mW)			**Stimulated power** (mW)	
	DVdd	AVdd	Total (no stimulus)	Added DVdd	Total (stimulated)
Sender	3.5	0.4	3.9	1.8	5.7
AB receiver	3.7	0.5	4.2	0.2	4.4
BL receiver	3.7	0.5	4.2	0.2	4.4
HR receiver	3.7	0.5	4.2	0.2	4.4

Additionally, for a fair comparison it must be noted that both the multichip and monolithic custom VLSI versions perform motion processing at a bandwidth of around 100 Hz, providing an effective 200 frames/s sampling rate which could be used for closed-loop control.

The size of each sender chip pixel could be reduced by alternating pixels with positive and negative response rather than by having each pixel respond to both signs of intensity change. This approximation would be particularly effective with large array sizes. However, at low array sizes, better performance will be obtained by colocating these two responses. A further improvement upon using two sender interface circuits per pixel would be to detect the sign of intensity change and direct it to the appropriate AER address, utilizing only a single sender interface circuit.

In addition to the motion outputs which have been the primary subject of this paper, a large amount of other vision data is available from the multichip vision processor. The sender chip raw photoreceptor values can be scanned out and a visual image constructed. In addition to the use of a motion receiver chip, a simpler receiver chip that merely integrates spike trains can be used to provide a "change-detection image," which shows only those parts of the image which change. Finally, using the fact that the output of each motion pixel is a current, the scanners on each motion receiver chip can be used to sum selected subregions of each chip, and provide global motion information. Due to the design of these scanners [29], two disjoint subregions can be provided simultaneously. The availability of all of this vision data from a compact custom VLSI vision system will allow extremely small autonomous robots to have powerful visual capabilities.

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REFERENCES

[1] J. Tanner and C. Mead, "An integrated analog optical motion sensor," in *VLSI Signal Processing II*, S.-Y. Kung, R. Owen, and G. Nash, Eds. New York: IEEE Press, 1986, pp. 59–76.

[2] J. Hutchinson, C. Koch, J. Luo, and C. Mead, "Computing motion using analog and binary resistive networks," *IEEE Computer*, vol. 21, no. 3, pp. 52–63, Mar. 1988.

[3] T. Horiuchi, J. Lazzaro, A. Moore, and C. Koch, "A delay-line based motion detection chip," in *Advances in Neural Information Processing Systems*, R. P. Lippman, J. E. Moody, and D. S. Touretzky, Eds. San Mateo, CA: Morgan Kaufmann, 1991, pp. 406–412.

[4] T. Delbrück, "Silicon retina with correlation-based, velocity-tuned pixels," *IEEE Trans. Neural Netw.*, vol. 4, no. 3, pp. 529–541, May 1993.

[5] J. Kramer, "Compact integrated motion sensor with three-pixel interaction," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 18, no. 4, pp. 455–460, Apr. 1996.

[6] X. Arreguit, F. A. van Schaik, F. Bauduin, M. Bidiville, and E. Raeber, "A CMOS motion detector system for pointing devices," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1916–1921, Dec. 1996.

[7] R. Sarpeshkar, J. Kramer, G. Indiveri, and C. Koch, "Analog VLSI architectures for motion processing: From fundamental limits to system applications," *Proc. IEEE*, vol. 84, no. 7, pp. 969–987, Jul. 1996.

[8] A. Moini, A. Bouzerdoum, K. Eshraghian, A. Yakovleff, X. T. Nguyen, A. Blanksby, R. Beare, D. Abbott, and R. E. Bogner, "An insect vision-based motion detection chip," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 279–283, Feb. 1997.

[9] R. Etienne-Cummings, J. Van der Spiegel, and P. Mueller, "A focal plane visual motion measurement sensor," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, no. 1, pp. 55–66, Jan. 1997.

[10] C. M. Higgins, R. A. Deutschmann, and C. Koch, "Pulse-based 2-D motion sensors," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 677–687, Jun. 1999.

[11] A. Torralba and J. Herault, "An efficient neuromorphic analog network for motion estimation," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 2, pp. 269–280, Feb. 1999.

[12] R. Etienne-Cummings, J. Van der Spiegel, and P. Mueller, "Hardware implementation of a visual-motion pixel using oriented spatiotemporal neural filters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 9, pp. 1121–1136, Sep. 1999.

[13] R. R. Harrison and C. Koch, "A robust analog VLSI Reichardt motion sensor," *Anal. Integr. Circuits Signal Process.*, vol. 24, pp. 213–229, 2000.

[14] S. C. Liu, "A neuromorphic aVLSI model of global motion processing in the fly," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, pp. 1458–1467, Dec. 2000.

[15] A. A. Stocker, "Analog VLSI focal-plane array with dynamic connections for the estimation of piecewise-smooth optical flow," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 5, pp. 963–973, May 2004.

[16] C. M. Higgins, V. Pant, and R. Deutschmann, "Analog VLSI implementations of spatio-temporal frequency based visual motion algorithms," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, to be published.

[17] C. M. Higgins and C. Koch, "A modular multichip neuromorphic architecture for real-time visual motion processing," *Anal. Integr. Circuits Signal Process.*, vol. 24, no. 3, Sep. 2000.

[18] K. Boahen, "Point-to-point connectivity between neuromorphic chips using address events," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 5, pp. 416–434, May 2000.

[19] E. H. Adelson and J. R. Bergen, "Spatiotemporal energy models for the perception of motion," *J. Opt. Soc. Amer. A*, vol. 2, no. 2, pp. 284–299, 1985.

[20] B. Hassenstein and W. Reichardt, "Systemtheorische analyze der Zeit-, Reihenfolgen- und Vorzeichenauswertung bei der Bewegungsperzeption des Rüsselkäfers *Chlorophanus*," *Z. Naturforsch.*, vol. 11b, pp. 513–524, 1956.

[21] H. B. Barlow and W. R. Levick, "The mechanism of directionally selective units in rabbit's retina," *J. Physiol.*, vol. 178, pp. 477–504, 1965.

[22] C. M. Higgins and S. A. Shams, "A biologically inspired VLSI system for visual measurement of self-motion," *IEEE Sensors J.*, vol. 2, no. 3, pp. 508–528, Jun. 2002.

[23] K. Boahen, "Retinomorphic chips that see quadruple images," in *Proc. 7th Int. Conf. Microelectronics for Neural, Fuzzy Bio-inspired Systems*, Apr. 1999, pp. 12–20.

[24] G. Indiveri, A. M. Whatley, and J. Kramer, "A reconfigurable neuromorphic VLSI multichip system applied to visual motion computation," in *Proc. 7th Int. Conf. Microelectronics for Neural, Fuzzy Bio-inspired Systems*, Apr. 1999, pp. 37–44.

[25] M. A. Mahowald, "VLSI analogs of neuronal visual processing: A synthesis of form and function," Ph.D. dissertation, Program in Computation and Neural Systems, California Institute of Technology, Pasadena, 1992.

[26] S. C. Liu, "Silicon retina with adaptive filtering properties," *Anal. Integr. Circuits Signal Process.*, vol. 18, no. 2/3, pp. 243–254, 1999.

[27] R. Sarpeshkar, R. F. Lyon, and C. A. Mead, "A low-power wide-dynamic-range analog VLSI cochlea," *Anal. Integr. Circuits Signal Process.*, vol. 16, no. 3, pp. 245–274, 1998.

[28] C. M. Higgins and C. Koch, "Multi-chip neuromorphic motion processing," in *Proc. 20th Conf. Advanced Research in VLSI*, Atlanta, GA, 1999.

[29] C. A. Mead and T. Delbrück, "Scanners for visualizing activity of analog VLSI circuitry," *Anal. Integr. Circuits Signal Process.*, vol. 1, pp. 93–106, 1991.

[30] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbruck, R. Douglas, and C. A. Mead, *Analog VLSI: Circuits and Principles*. Cambridge, MA: MIT Press, 2002.

[31] C. M. Higgins and S. K. Korrapati, "An analog VLSI motion energy sensor based on the Adelson-Bergen algorithm," in *Proc. Int. Symp. Biologically Inspired Systems*, Wollongong, Australia, Dec. 2000.
[32] A. G. Andreou and K. A. Boahen, "Translinear circuits in subthreshold MOS," *Anal. Integr. Circuits Signal Process.*, vol. 9, pp. 141–166, 1996.
[33] R. G. Benson and T. Delbrück, "Direction selective silicon retina that uses null inhibition," in *Advances in Neural Information Processing Systems 4*, D. S. Touretzky, Ed. San Mateo, CA: Morgan Kaufmann, 1991, pp. 756–763.
[34] A. G. Andreou and K. Strohbehn, "Analog VLSI implementation of the Hassenstein-Reichardt-Poggio model for vision computation," in *Proc. IEEE Int. Conf. Systems, Man, Cybernetics*, Los Angeles, CA, Nov. 1990, pp. 708–710.
[35] R. Sarpeshkar, W. Bair, and C. Koch, "An analog VLSI chip for local velocity estimation based on Reichardt's motion algorithm," in *Advances in Neural Information Processing Systems 5*, S. J. Hanson, J. Cowan, and L. Giles, Eds. San Mateo, CA: Morgan Kaufmann, 1993, pp. 781–788.
[36] S. C. Liu, "Neuromorphic models of visual and motion processing in the fly visual system," Ph.D. dissertation, Program in Computation and Neural Systems, California Institute of Technology, Pasadena, CA, 1997.
[37] M. Egelhaaf and A. Borst, "Transient and steady-state response properties of movement detectors," *J. Opt. Soc. Amer. A*, vol. 6, pp. 116–127, 1989.
[38] C. C. Chang and S. I. Liu, "Weak inversion four quadrant multiplier and two-quadrant divider," *Electron. Lett.*, vol. 34, 1998.

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